Electro-Thermal simulation study of MOSFET modeling in Silicon and Silicon carbide

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ABSTRACT

In this paper, a 2D electro-thermal coupling model of a MOSFET power device is presented using COMSOL Multiphysics software. The main objective of the model is to investigate and analyze the effect of temperature change on the electrical characteristics of a lateral MOSFET, visualize the heat distribution throughout the device, and calculate the peak temperature reached under extreme conditions. Thus, a comparison study is performed between Si and 6H-SiC based devices to highlight the effect of device material on its performance. The temperature distribution and the maximum temperature reached in both Si, and 6H-SiC MOSFETs evaluate the reliability of the power component. The obtained results reveal lower drain currents and hot spot temperature values 4% to 8% lower in 6H-SiC MOSFET.

1. INTRODUCTION

Most of the electronic components such as transistors, resistors, capacitors, diodes, and integrated circuits, generate heat when used in an electronic system but can withstand specific amounts of heat. However, different internal and external situations can result in overheating that can potentially damage the electronic component. The high external temperature circumstances or generated by self-heating creates significant electro-thermal stress. This can defect the metallization, bonding wire lift, and progressively result in device failure and breakdown [1]. Several studies have investigated the overheating problems' causes and heat distribution in several applications [2]. Reference [3] conducted numerical-simulation experiments to investigate the effect of the viscous heat dissipation and compression work on the temperature distribution. Other research works reported heat distribution and its impact on fluids [4, 5]. Self-healing is an essential issue for smart devices and power ICs requiring more stability at high temperatures. Indeed, many studies have presented the effect of temperature on the electrical properties of a MOSFET transistor using different models [6]–[9]. However, simulations of electrical properties and temperature distribution throughout different MOSFETs' materials based on extreme temperature conditions have not been investigated clearly.

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Silicon (Si) based devices have theoretical and practical limitations for high-temperature applications (MOSFETs and CMOS technology). The intrinsic requirements of semiconductor materials (high thermal conductivity, large breakdown voltage, high electron mobility, significant saturated electron drift velocity, small dielectric constant, and small on-resistance) for high power and high-temperature applications cannot be fulfilled by silicon. The maximum tolerable operating temperature for silicon devices is around 150°C [10]–[12]. Silicon carbide (SiC) is an alternate material whose properties make it suitable for use in more extreme environments. Table 1 presents a comparison between Si and SiC properties [13].

Table 1: Si and SiC material properties comparison

Properties	Si	6H-SiC
Band gap (eV)	1.1	2.9
Dielectric constant	11.8	9.7
Breakdown field (V/cm)	6×105	35×105
Saturated velocity (cm/s)	1 ×107	2×107
Electron mobility (in bulk) (cm2/V s)	1350	380
Hole mobility (in bulk) (cm2/V s)	450	95
Thermal conductivity (W/cm K)	1.5	4.9
Melting point (°C)	1420	2830

Recently, silicon carbide (SiC) has demonstrated excellent performance in high-temperature stability than conventional semiconductor materials such as silicon (Si) and gallium arsenide (GaAs) due to its wide bandgap. Additionally, it possesses a high breakdown field, and the capability to produce SiO2 gate insulators simply by thermal oxidation of the surface. Therefore, silicon carbide (SiC) is an ideal material for high-power and high-temperature electronic devices. Besides, SiC has many advantages over other wide bandgap semiconductors. This makes the material as a promising material for many high-temperature applications (space exploration industries, geothermal explorations, and automotive engine control) and leads to significant cost savings in packaging and cooling systems (aircraft, shipboard, and hybrid vehicle applications). Moreover, SiC MOSFETs are more suitable for monolithic smart power ICs due to their stability at high temperatures and moderate speed [14]–[16]. 6H-SiC is ideal in the parallel direction in 6H-SiC [17], [18].

This paper presents a comparative study of the electro-thermal behavior on the state of lateral MOSFETs for Si and 6H-SiC based devices using COMSOL Multiphysics, a reliable simulation tool. This simulation tool has been used to investigate electrical, mechanical, and thermal properties in different applications [19]-[22]. A study of the device temperature change on the electrical behavior of the power device and the temperature distribution throughout the device is presented and discussed. The maximum temperature values obtained from this electro-thermal simulation are required to evaluate the reliability of the power device.

2. ELECTRO-THERMAL COUPLING MODEL

The presented MOSFET model is a miniaturized switch (Fig.1). In the COMSOL software model, the device length L and width W are set to be 3 μm. The source and the drain contacts are both ohmic. These regions are heavily doped n-type silicon with a peak concentration of $1x10^{20}\ cm^{-3}$ and a Gaussian drop off with a junction depth of $0.25\ \mu m$. Between these two contacts, a region of p-type silicon is assumed to have a concentration of $1x10^{17}\ cm^{-3}$. The gate contact above the p-type region is separated from the semiconductor by a thin layer of Silicon dioxide.

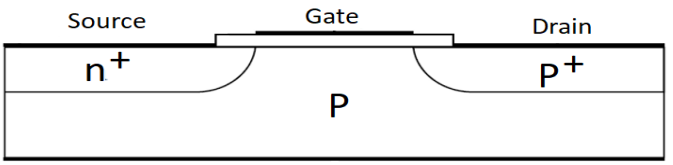


Fig. 1. Schematic diagram of a typical MOSFET

The Shockley-Read-Hall recombination model is implemented in a trap-assisted recombination feature to capture the main recombination effect.

The studied model represents a coupling between the semiconductor interface and the heat transfer at the interface of the solid in order to calculate the temperature distribution throughout the device for the different gate voltage V_g, drain voltage V_d, device material and device temperature. This model includes the effects of a non-uniform temperature and calculates the maximum hot spot temperature reached in the device. The electrical and thermal simulations are completed and performed in a stationary mode study in COMSOL. The Physics of the two studies is fully coupled by selecting the solution of the semiconductor study as an initial condition for the heat transfer study.

The heating throughout the model, defined as Semi.Q_tot variable, is calculated by COMSOL semiconductor interface then configured as the heat source in the heat transfer in solids interface. The temperature distribution, defined as the T variable, is calculated by the heat in solids interface then fed back in the semiconductor interface into the material temperature via a second semiconductor material model node. The first semiconductor material model node uses a constant material temperature. The heat flux q_0 between the model and its environment (1) over the total area A of the contact, boundaries are studied via convection. The contact boundaries heat transfer coefficient h_0 is shown in (2):

$$q_0 = h_0(T - T_0) \tag{1}$$

$$h_0 = \frac{1}{R.A} = \frac{1}{R.(W.L)} \tag{2}$$

where W and L are the width and length of the metal contacts respectively, R is the effective thermal resistance, h_0 represents the effect of an exterior fluid cooling or heating the surface of a solid, and T is the external temperature surrounding the modeled domain. The semiconductor interface is configured to use an incomplete ionization model for the dopant ionization. Incomplete dopant ionization is an important temperature-dependent process that affects the carrier concentration, and thus currents, through the semiconductor material. An automatic tessellation mode defines a user-controlled mesh for the entire geometry. A mapped domain setting is applied to the top surface of the device to adjust the mesh edge with a maximum element size of 30 nm. A free triangular mesh is defined for the rest, with maximum and minimum element sizes of 39 nm and 6 nm, respectively. The maximum element growth rate is set to 1.05 with a curvature factor of 0.3.

3. HEAT EFFECT ON THE ELECTRICAL AND THERMAL BEHAVIOR OF THE POWER DEVICE

Since the threshold voltage V_{th} is the most significant parameter while sthe tudy of the temperature dependence of MOSFET characteristics, the effect of the temperature variation on the threshold voltage V_{th} and the drain current Id are presented respectively for both Si and 6H-SiC based devices. While in saturation, the current–voltage characteristics are proportional to the square of the difference between gate voltage and threshold voltage, as given in equation (3) below.

$$I_d \approx \frac{W.\mu.C_{ox}}{2.L}\left(V_g - V_{th}\right)^2 \tag{3}$$

where μ and C_{ox} are the carrier mobility and the oxide capacitance per unit area, respectively. Two studies are investigated the COMSOL semiconductor interface. In the first study, the model sweeps the voltage applied to the gate contact V_g whilst the drain contact is held at a constant voltage of $V_d = 4\,V$ (to operate in saturation region). The main purpose of this study is to evaluate the threshold voltage and its variation with temperature. In the second study, the model sweeps the voltage applied to the drain contact V_d whilst the gate contact is held at a constant voltage $V_g = 4V$ (higher than the threshold voltage) Thus, the $I_d - V_d$ characteristics can be evaluated for different temperatures. The values of the drain current in saturation and the carries mobility can then be estimated. Figs. 2 and 3 show, respectively, the variation of $\sqrt{I_d}$ vs. V_g for Si and 6H-SiC based devices for temperatures 293 K,500 K and 700 K. The threshold voltage values obtained are given in the Table 2.

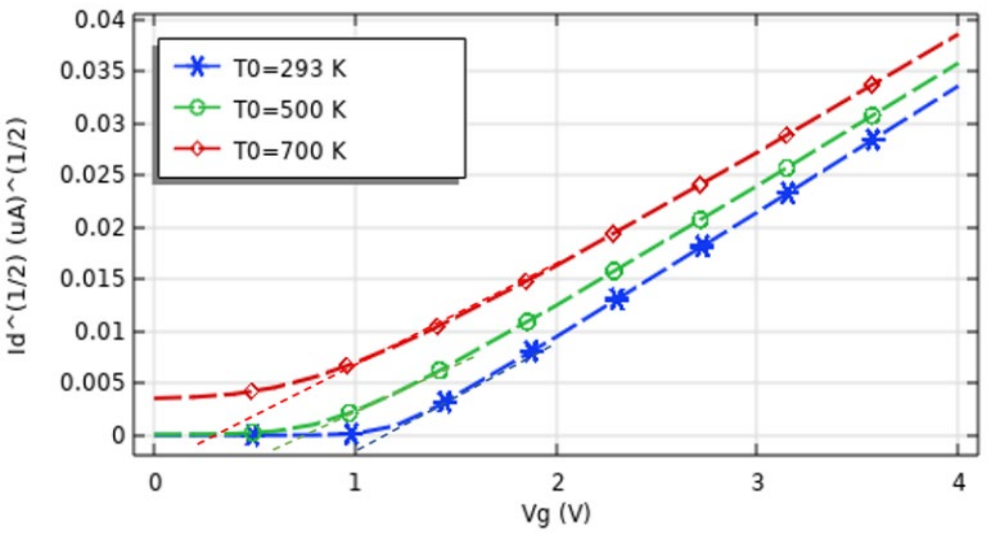


Fig. 2. Square root of drain current vs. gate voltage for a Si based device

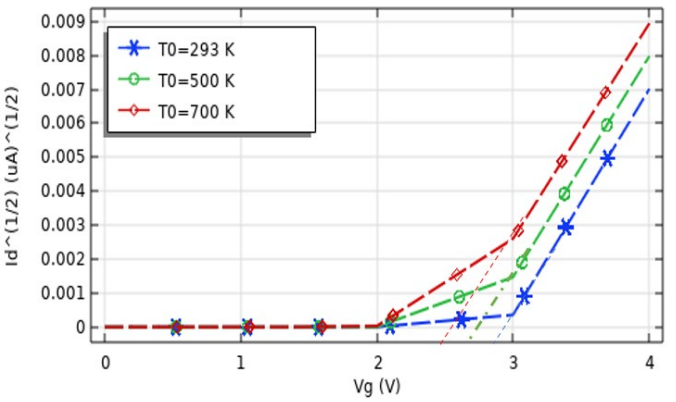


Fig. 3. Square root of drain current vs. gate voltage for a 6H-SiC based device.

Table 2 Threshold values for Si and 6H-SiC based device

	Threshold Voltage V_{th}(V)		
Temperature (K)	293	500	700
Si	0.9	0.5	0.2
6H-SiC	2.9	2.7	2.5

One can notice that the threshold voltage decreases with increasing the temperature. The observed behavior agrees well with the previous experimental result, e.g. [14], [15]. This is due to a change in charge held in interface states as the Fermi level changes its position with temperature. Vth is a function of the reverse of the intrinsic carrier's concentration, which increases linearly with temperature [10], [11]. Also, the generation process of oxide-trapped charges and impurities at the Si/SiO_2 interface is thermally activated; thus, it produces interface states and the distribution of oxide defects near the interface [12]. As a result, Vth decreases at high temperatures [13], [14]. However, the value obtained for the threshold voltage for Si based device at 700 K (0.2 V) is dangerously close to the gate drive turn-off potential, which is not the case for 6H-SiC based device. This clearly shows the high impact of the extreme temperature on the Si based device.

The drain current I_d versus drain voltage V_d characteristics are then studied with Vg=4V for Si and 6H-SiC based devices, for different temperatures 293 K, 500 K, and 700 K. the obtained results are presented in figures 4 and 5, respectively. The linear and saturation (pinch-off) regions for the device can be identified from these curves.

The values of the drain saturation current I_{Dsat} deduced from the curves at VDS = 7 V (in the saturation region) for different temperatures are collected in Table 3 for both Si and 6H-SiC based devices. The variation of the saturation current shows clearly that I_{Dsat} increases with temperature. Indeed, the decrease of Vth with temperature leads to an establishment of the current in the channel at lower gate voltage and an earlier strong inversion. For a given gate voltage, the channel and therefore, the saturation current becomes more significant as the temperature increases. This is in accordance with results obtained in an experimental work investigating on the temperature effect on a commercial VDMOSFET transistor [23].

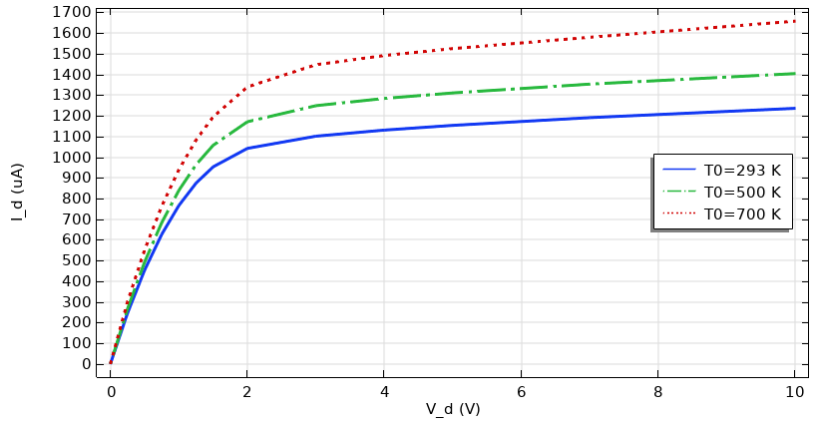


Fig. 4. Drain current versus drain voltage for a Si based device for different temperatures.

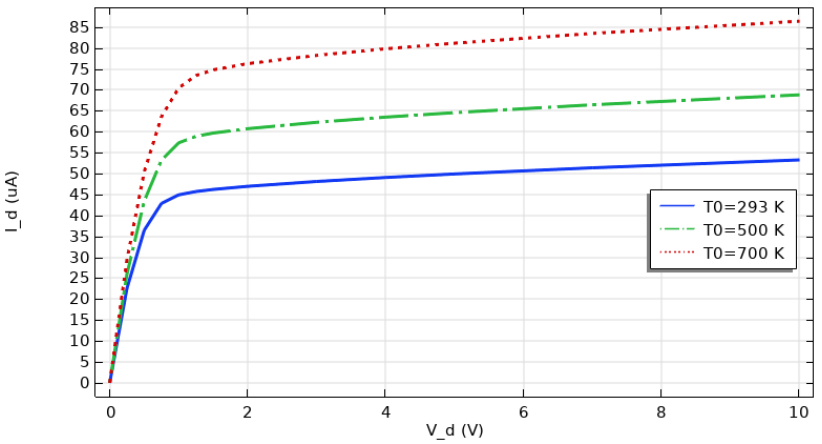


Fig. 5. Drain current versus drain voltage for a 6H-SiC based device for different temperatures.

Table 3 Drain saturation current I_{Dsat} (μA) for Si and 6h-SiC based device

	Drain saturation current I_{Dsat}		
Temperature (K)	293	500	700
Si	1190.9	1353.1	1579.5
6H-SiC	51.373	66.432	83.480

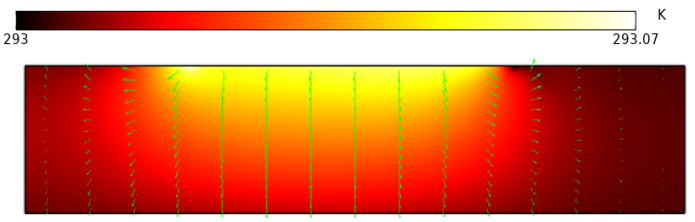
Table 4 Carrier's mobility k.μ (F/V.s)

Temperature (K)	293	500	700
Si	$1.24x10^{-4}$	$1.10x10^{-4}$	$1.09x10^{-4}$
6H-SiC	$4.24x10^{-5}$	$3.93x10^{-5}$	$3.71x10^{-5}$

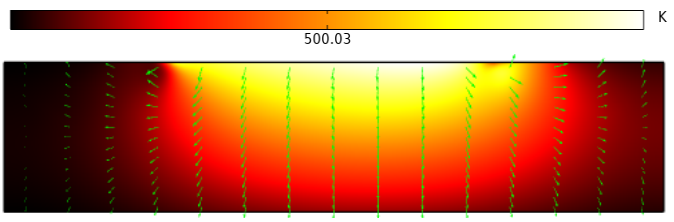
For a Si-based device, the drain current increases by 12 % at T=500 K and by 24.6 % at T=700 K, compared to the drain current at T=293 K. For a 6H-SiC based device, the drain current is increased by 22.7 % at T=500 K and by 38.5 % at T=700 K compared to the drain current at T=293 K. These results clearly show the effect of the temperature on the drain current for both Si and 6H-SiC based devices. However, minimum values of drain currents (up to 90 %) in the saturation region are obtained in the 6H-SiC based device compared to the Si-based device for different temperatures (293 K, 500 K, 700 K) and the same gate voltage. By considering W, L and C_{ox} in equation (3) constants with temperature. Given the values of V_g, V_{th} and I_{Dsat}, we can estimate the value of carrier's mobility μ at each temperature (Table 4) with $k = \frac{W.C_{ox}}{2L}$.

It can be concluded that the carrier's mobility μ is clearly decreasing with temperature. The approximate mobility-temperature dependence is $T^{-\frac{3}{2}}$ for lattice scattering [15]. We can state also that the carrier's mobility in 6H-SiC based device is 10 times smaller than that in Si based device, which verifies the smaller values of current obtained for 6H-SiC based device at different temperatures.

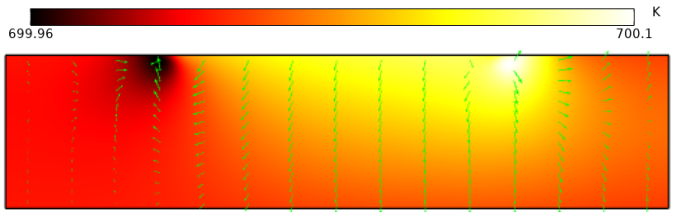
To investigate on this, temperature distribution throughout the Si and 6H-SiC based device is studied for different external temperatures 293 K, 500 K, and 700 K in order to locate the hottest spot and calculate its temperature. The surface plot in Figures 6 and 7 depicts the temperature distribution throughout the Si-based device, along with an arrow plot that shows the heat flux distribution.



a. T0=293 K

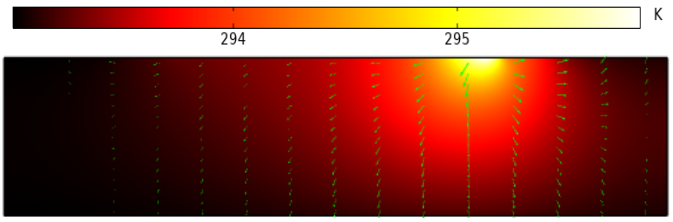


b. T0=500 K

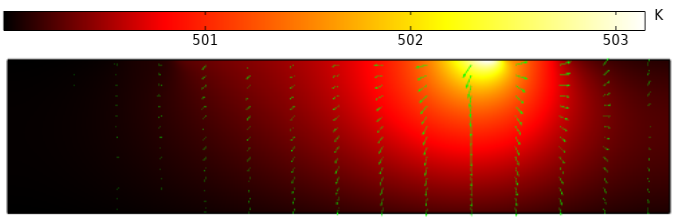


c. T0=700 K

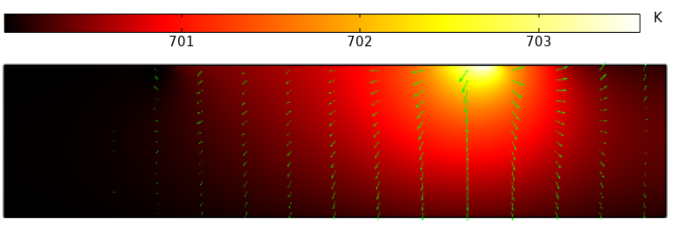
Fig. 6. Temperature distribution throughout the device for V_d=0.5 V and for different temperatures (a: T0=293 K, b: T0=500 K, c: T0=700 K)



a. T0=293 K



b. T0=500 K



c. T0=700 K

Fig. 7. Temperature distribution throughout the device for Vd=4 V and for different temperatures (a: T0=293 K, b: T0=500 K, c: T0=700 K)

For a fixed gate voltage of 4 V and a low drain voltage of 0.5 V, the results show a heated region confined under the gate contact at T=293 K. This heat source region is more intense at T=500 K and shifts to the drain contact at T=700 K (Fig.6). The temperature calculated in the device is approximately the same external temperature, which is expected, since for such low drain voltage ($V_d = 0.5V$) the drain current is low enough to not result in any self-heating of the device. However, when the drain voltage is increased to 4V (Fig.7), hotspot occurs under the gate edge looking to the drain side due to highly localized heat generation. This hotspot is localized in the same region for all studied temperatures (T=293,500 and 700 K).

This is a logical result as once the inversion layer is formed by increasing the drain voltage, the majority of the current flows between the drain and source contacts, and a region is created between the gate and the drain contacts with higher resistance than the surrounding bulk material. In fact, as the temperature increases, more electrons are available to be drawn to the channel. Existing interface traps will also have energies closer to the conduction band to reduce resultant channel resistance, leading to a faster accumulation of electrons in the channel. Thus, the Joule heating, the predominant semiconductor heating mechanism in this model, is the largest in this location. The heat flux also behaves as expected, as it flows from the peak temperature towards the contacts, the only boundaries allowing the heat transfer in this model.

The same study is repeated for the 6H-SiC based device. The same temperature distribution behavior is obtained. The hot spot (heat source) is located at the same gate-drain junction region. Please note that this is not the temperature of the complete and packaged part. It is only the junction temperature, the hottest spot. For a Si and 6H-SiC based device, at $V_d = 10\ V$, $V_g = 10\ V$, $T_0 = 700\ K$ and $L = 10\ \mu m$, the temperature profile along the device are plotted and represented respectively in figures 8 and 9, at several locations from the top surface. This plot illustrates the heat source location in the device and the maximum temperature variation based on the location from the device top surface. One can observe that maximum internal temperature is obtained at a location close to the device's top surface, at the heat source location. This maximum temperature decreases as far as we go from the top surface until reaching the device's bottom surface.

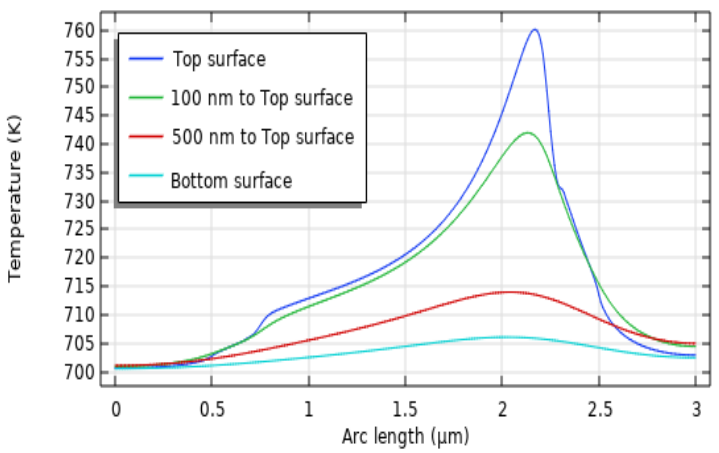


Fig. 8. Temperature profile plot along the device at several locations from the device top surface for a Si based device.

The simulation results for the Si-based device show that, for $V_g = 10\ V$ and $V_d = 10\ V$, the maximum hotspot reached temperature is 322 K for $T_0 = 293\ K$, 530 K for $T_0 = 500\ K$ and 732 K for $T_0 = 700\ K$.

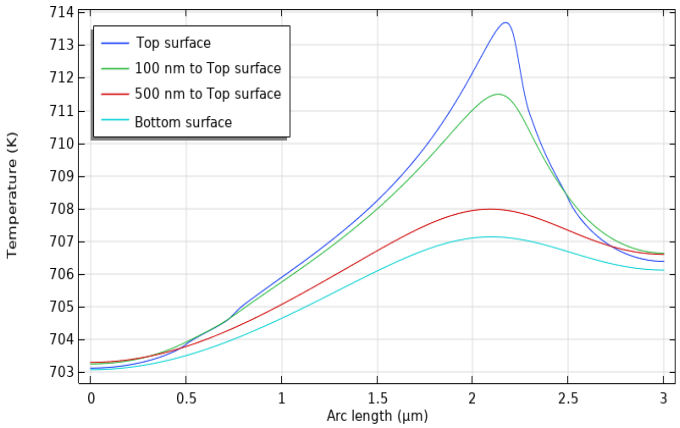


Fig. 9. Temperature profile plot along the device at several locations from the device top surface for a 6H-Sic based device

For 6H-SiC based device, calculations show that for $V_g = 10\ V$ and $V_d = 10\ V$, the maximum hotspot reached temperature is 297 K for $T_0 = 293\ K$, 504 K fot $T_0 = 500\ K$ and 705 K for $T_0 = 700\ K$. These results reveal that lower internal temperatures have been obtained in the 6H-SiC based device compared to the Si-based device by 7.7 % for $T_0 = 293\ K$, 5 % for $T_0 = 500\ K$ and 3.7 % for $T_0 = 700\ K$. Therefore, the self-heating effect is lower in the 6H-SiC than in the Si-based device. Such results reflect the importance of the 6H-SiC material compared to Si material in MOSFET power devices since silicon carbide material SiC has a relatively higher thermal conductivity and thus reduces the hot spot temperature in the device.

4. CONCLUSION

This paper presents a finite element model of the MOSFET transistor. A simulation study of the external temperature effect on the threshold voltage, drain current, temperature distribution, and the maximum temperature reached throughout the device has been presented for Si and 6H-SiC MOSFETs. Results show lower drain current values obtained in the 6H-SiC than in the Si-based devices for different gate voltages and external temperatures. Moreover, the temperature distribution study describes the appearance of a region localized under the gate and shifts to the drain contact side by increasing the voltage. It was found that hot spot temperatures for a Si MOSFET are 4 % to 8 % higher than in 6H-SiC MOSFET. This research paper has shown that the material device choice has the simple impact of biasing the maximum temperature in the device. Higher temperatures within the device are observed when a substrate with lower thermal conductivity is used, like in Si. Therefore, SiC MOSFETs are more suitable and reliable for extreme environments.

REFERENCES

[1] R. Amro, J. Lutz, J. Rudzki, R. Sittig, and M. Thoben, "Power cycling at high temperature swings of modules with low temperature joining technique," Proceedings of the International Symposium on Power Semiconductor Devices and ICs, vol. 2006, 2006.

[2] Chow, K., & Holdø, A. Numerical prediction of indoor temperature stratification. "The International Journal of Multiphysics", vol. 2, no. 4, pp. 355-366, 2008.

[3] Ren, X., Liu, F., Wang, S., & Wei, S. Numerical Study of the Effect of Viscous Heat Dissipation and Compression Work on Microscale Rayleigh–Bénard Convection Based on a Coupled Thermal Lattice Boltzmann Method. "The International Journal of Multiphysics", vol. 12, no. 2, pp. 101-116, 2018.

[4] Hona, J. Modeling of heat and high viscous fluid distributions with variable viscosity in a permeable channel. "The International Journal of Multiphysics", vol. 9, no. 4, pp. 341-360, 2015.

[5] Azri, K., Mezaache, E., & Mecili, M. Thermal Transfer Study of a Non-Newtonian Nanofluid Behavior in a Microduct. "The International Journal of Multiphysics", vol. 16, no. 3, pp. 235-259, 2022.

[6] S. Tiwari, S. Dolai, H. Rahaman, and P. S. Gupta, "Effect of temperature & phonon scattering on the drain current of a MOSFET using SL-MoS2 as its channel material," Superlattices and Microstructures, vol. 111, pp. 912–921, Nov. 2017.

[7] F. Echouchene and H. Belmabrouk, "Effect of temperature jump on nonequilibrium entropy generation in a MOSFET transistor using dual-phase-lagging model," Journal of Heat Transfer, vol. 139, no. 12, Dec. 2017.

[8] J. Y. Wu, P. W. Sze, Y. H. Wang, and M. P. Houng, "Temperature effect on gate leakage currents in gate dielectric films of GaAs MOSFET," Solid-State Electronics, vol. 45, no. 12, pp. 1999–2003, Dec. 2001.

[9] H. Takeda, M. Sometani, T. Hosoi, T. Shimura, H. Yano, and H. Watanabe, "Insight into channel conduction mechanisms of 4h-sic (0001) mosfet based on temperature-dependent hall effect measurement," Materials Science Forum, vol. 1004 MSF, pp. 620–626, 2020.

[10] J. M. Early, "High-Temperature Diffusion Leakage-Current-Dependent MOSFET Small-Signal Conductance," IEEE Transactions on Electron Devices, vol. 31, no. 12, pp. 1866–1872, 1984.

[11] "Design considerations in high temperature analog CMOS integrated circuits," Microelectronics Reliability, vol. 27, no. 4, p. 790, Jan. 1987.

[12] F. S.-E. Letters and undefined 1987, "CMOS logic cell switching speed thermal characterisation," IET, Accessed: Jul. 14, 2021. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/el_19870331

[13] C. E. Weitzel et al., "Silicon carbide high-power devices," IEEE Transactions on Electron Devices, vol. 43, no. 10, pp. 1732–1741, 1996.

[14] R. F. Davis, G. Kelner, M. Shur, J. A. Edmond, and J. W. Palmour, "Thin Film Deposition and Microelectronic and Optoelectronic Device Fabrication and Characterization in Monocrystalline Alpha and Beta Silicon Carbide," Proceedings of the IEEE, vol. 79, no. 5, pp. 677–701, 1991.

[15] H. M. Hobgood et al., "Large diameter 6H-SiC for microwave device applications," Journal of Crystal Growth, vol. 137, no. 1–2, pp. 181–186, Mar. 1994.
[16] S. Ryu, K. T. Kornegay, J. A. Cooper, and M. R. Melloch, "Monolithic CMOS digital integrated circuits in 6H-SiC using an implanted p-well process," IEEE Electron Device Letters, vol. 18, no. 5, pp. 194–196, May 1997.
[17] N. Rebello, … F. S.-I. P.-C., and undefined 1996, "6H silicon carbide MOSFET modelling for high temperature analogue integrated circuits (25-500/spl deg/C)," ieeexplore.ieee.org, Accessed: Jul. 14, 2021. [Online]. Available: https://ieeexplore.ieee.org/document/494180/
[18] "Development of CMOS technology for smart power applications in silicon carbide - ProQuest."https://www.proquest.com/docview/304380301?pqorigsite=gscholar&fromopenview=true (accessed Jul. 13, 2021).
[19] Brunner, D., Khawaja, H., Moatamedi, M., & Boiger, G. CFD modelling of pressure and shear rate in torsionally vibrating structures using ANSYS CFX and COMSOL Multiphysics. "The International Journal of Multiphysics", vol. 12, no. 4, pp. 349-358, 2018.
[20] Mourched, B., & Abdallah, M. Design and characterization of a new microscopy probe using COMSOL and ANSYS. "The International Journal of Multiphysics", vol. 16, no. 1, pp. 95-106, 2022.
[21] Jourdani, M., Mounir, H., & Marjani, A. Three-Dimensional PEM Fuel Cells Modeling using COMSOL Multiphysics. "The International Journal of Multiphysics", vol. 1, no. 4, pp. 427-442, 2017.
[22] Missoum, A., Elmir, M., Bouanini, M., & Draoui, B. Numerical simulation of heat transfer through the building facades of buildings located in the city of Bechar. "The International Journal of Multiphysics", vol. 10, no. 4, pp. 441-450, 2016.
[23] N. Abboud, C. Salame, Y. Cuminal, A. Foucaran, and A. Hoffmann, "Temperature effect on an N-channel commercial VDMOSFET transistor," Physica Status Solidi (C) Current Topics in Solid State Physics, vol. 8, no. 3, pp. 875–878, Mar. 2011.