International Journal of Multiphysics
Volume 18, No. 4, 2024
ISSN: 1750-9548

A Low Power Recycling Folded Cascode OTA for Medical Applications

Mohammadreza Farsi[1], Ali Soleimani[1], Hadi Grailu[1]

[1]Department of Electrical and Robotics Engineering, Shahrood University of Technology, Shahrood, Iran

Abstract

A low power recycling folded cascode OTA which utilizes a novel CMRR magnifier block (CMRFC OTA) is presented in this paper. Incorporating the CMRR magnifier block helps to yield higher CMRR values while eliminating cascode structure. DC bias voltage of the cascode stage is eliminated accordingly. This interestingly leads to a low voltage low power design. The bias current is reduced in the proposed OTA which effectively reduces power consumption. A satisfactory phase margin is achieved for presented OTA which can be further improved incorporating the compensation resistor to isolate NMOS current mirrors parasitic capacitors. Low power CMRFC amplifier is simulated in 180nm CMOS technology with a 1.5 v supply voltage. The simulation results prove better performance of the structure in comparison with other works. The proposed OTA has a gain and phase margin of 54.1dB and 87.16 degree, respectively. The bias current and power consumption are 7.2 µA and 8.45 µw, respectively.

Keywords: Recycling folded cascode, CMRFC OTA, CMRR magnifier block, Low power.

1. Introduction

Transistor ratio scaling has significantly promoted low power microelectronic design in many fields, including analog circuits, control systems, instruments, medical and neural science [1]. In recent years, many efforts have been made to design a low power interface for neural recording systems [2].

If the amplitude of the acquired neural signals is lower than the required limit, it needs to be amplified before processing. For acceptable function of amplifiers in medical applications, it is essential to reduce power consumption as much as possible to eliminate body tissue damage caused by generated heat [3]. On the other hand, inspecting amplifier noise is important because noise represents the lower limit of the electrical signal that can be reconstructed without distortion [4].

In amplifiers, cascode structures are utilized to achieve high gain. Telescopic cascode amplifiers have low power consumption and noise; however, the swing is limited in these structures. Improvement in the output voltage swing in folded cascode amplifiers comes at the cost of increased power consumption and input noise. Additionally, the connection of input-output for buffer applications is much easier in folded cascode amplifiers, leading to their wider usage compared to telescopic structures [5].

In folded cascode amplifiers with NMOS differential input pairs, higher gain can be achieved compared to PMOS differential pairs. However, a smaller non-dominant pole will decrease the amplifier bandwidth. To increase gain and bandwidth, recycling folded cascode amplifiers (RFC) with trivial isolation of AC and DC current paths have been presented in [6]. Due to the inability to achieve full isolation of AC and DC current paths, transconductance in this structure has been limited as noted in [7]. Improved recycling folded cascode (IRFC) amplifiers have been designed to improve transconductance without increasing area and bias current. In [8], a conventional DRFC structure has been proposed in which the differential input pair has been replaced with triplet transistors. By reusing the shunt bias current in this structure, both gain and bandwidth have been improved. Folded cascode amplifiers designed in [6-10] have larger bandwidths but also much higher power consumption, making them unsuitable for today's low-power applications. In [11], a low-voltage, low-power technique to decrease power consumption and input reference noise has been introduced. Using this technique, power consumption has been

effectively decreased by reducing the supply voltage; however, the trade-off is a noticeable decrease in amplifier gain bandwidth. Additionally, this structure has not shown a considerable decrease in input reference noise.

In this article, an RFC amplifier based on a CMRR magnifier block has been proposed. Using this block, the common-mode current of the amplifier is omitted by utilizing NMOS transistors at the input stage. In this structure, power consumption and bias current have been decreased. A reassuring phase margin for this circuit has been achieved, and with the isolation of the parasitic capacitors, the phase margin can be further improved [12]. Another advantage of this structure is the decrease in bias current.

This article consists of the following sections: Section 2 is dedicated to the design and analysis of a low-power, low-voltage CMRFC (OTA). Simulation results will be presented in Section 3. Finally, the article will conclude with the representation of the conclusions.

2. Design and analysis of proposed CMRFC

In conventional RFC amplifiers, to increase in accuracy of signal transfer, cascode transistors were used. Cascode transistors caused an increase in amplifiers CMRR, but the cost was the need for a high voltage supply which resulted in increase of power consumption. Proposed low-power CMRFC amplifier is shown at Figure 1. In this structure, cascade transistors have been omitted and CMRR magnifier block has replaced. This block is shown in Figure1 with dashed. Replacing this block has the common mode current to be omitted at the input stage. Thus, circuit's CMRR is increased compared to the convention structures. Not only omitting the Cascode transistors has added the low voltage-low power feature to the amplifier, but also has omitted the DC bias voltage in cascode stage. Moreover, DC current bias has been significantly decreased which has a great effect in reduction of power consumption.

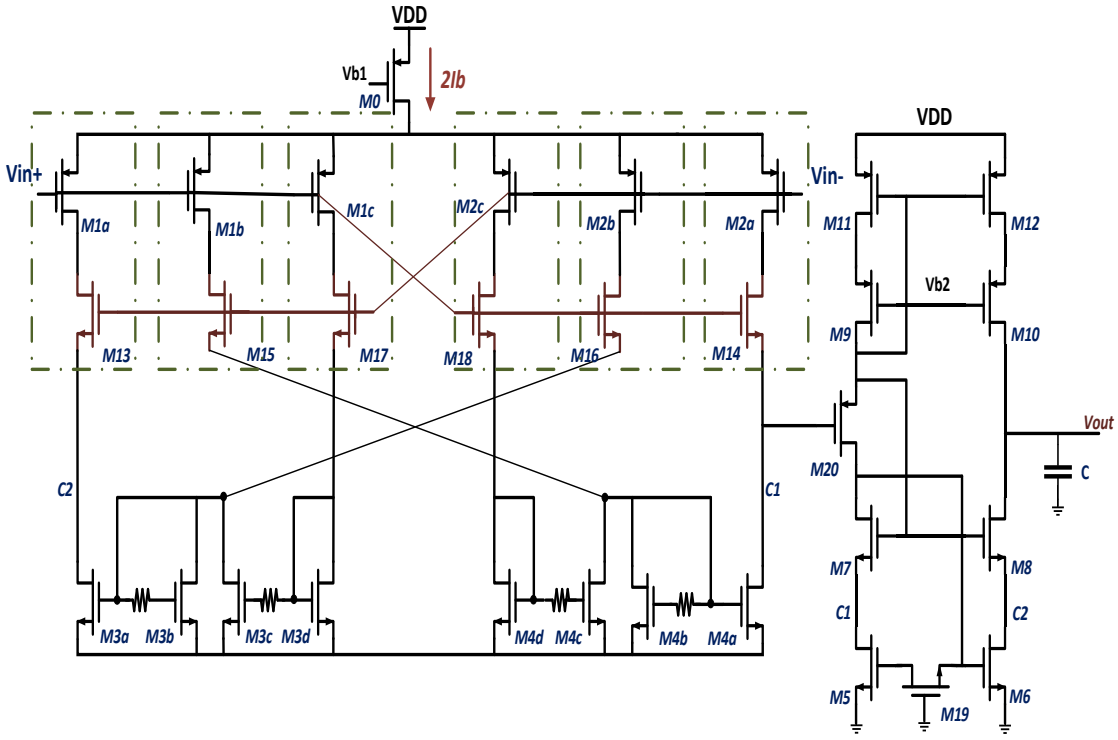


Figure 1.Proposed low power CMRFC OTA

To analyse circuit performance, the small-signal equivalent circuit is shown in Figure 2.

Using the transfer impedance of the input stage, *Rs* value can be written as follows:

$$R_{13} = \frac{h.rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}}{1+\mu_{13}}$$

$$R_{14} = \frac{h.rds_0(1+\mu_{2a}) + rds_{2a} + rds_{14}}{1+\mu_{14}}$$

$$R_{15} = \frac{h.rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}{1+\mu_{15}}$$

$$R_{16} = \frac{h.rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}{1+\mu_{16}} \quad (1)$$

$$R_{17} = \frac{h.rds_0(1+\mu_{1c}) + rds_{1c} + rds_{17}}{1+\mu_{17}}$$

$$R_{18} = \frac{h.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}}{1+\mu_{18}}$$

Which h for differential and common mode is zero and 1, respectively.

$$V_{13} = \frac{Vin_2\mu_{1a} - Vin_2\mu_{13}}{1+\mu_{13}}$$

$$V_{14} = \frac{Vin_1\mu_{2a} - Vin_2\mu_{14}}{1+\mu_{14}}$$

$$V_{15} = \frac{Vin_2\mu_{1b} - Vin_1\mu_{15}}{1+\mu_{15}}$$

$$V_{16} = \frac{Vin_1\mu_{2b} - Vin_2\mu_{16}}{1+\mu_{16}} \quad (2)$$

$$V_{17} = \frac{Vin_2\mu_{1c} - Vin_1\mu_{17}}{1+\mu_{17}}$$

$$V_{18} = \frac{Vin_1\mu_{2c} - Vin_2\mu_{18}}{1+\mu_{18}}$$

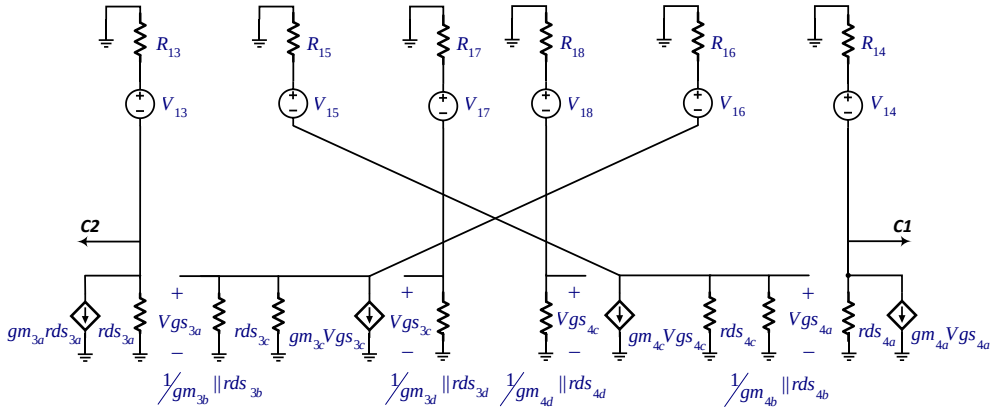


Figure 2.The small-signal equivalent circuits of CMRFC structure

For output stage, *C1* and *C2* nodes are two current paths. The current equation of the *C1* node according to Figure 2 can be written as follows:

$$I_x = gm_{4a} Vgs_{4a} + \frac{Vin_1 \mu_{2a} - Vin_2 \mu_{14}}{h.rds_0(1+\mu_{2a}) + rds_{2a} + rds_{14}} \tag{3}$$

That

$$Vgs_{4a} = [\frac{1}{gm_{4b}} \| rds_{4b} \| rds_{4c} \| R_{15}](gm_{4c} Vgs_{4c} + \frac{Vin_2 \mu_{1b} - Vin_1 \mu_{15}}{h.rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) \tag{4}$$

$$Vgs_{4c} = [\frac{1}{gm_{4d}} \| rds_{4d} \| R_{18}](\frac{Vin_1 \mu_{2c} - Vin_2 \mu_{18}}{h.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}}) \tag{5}$$

Finally, *Ix* can be in terms of *Vin1* and *Vin2* wrote:

$$I_x = Vin_1(F) - Vin_2(G) \tag{6}$$

That *F* and *G* are coefficients of *Vin1* and *Vin2*, respectively. Which are equal to:

$$F = [\frac{gm_{4a}}{gm_{4b}}(\frac{gm_{4c}\mu_{2c}}{gm_{4d} h.rds_0(1+\mu_{2c}) + (rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}} - \frac{\mu_{15}}{rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) + \frac{\mu_{2a}}{rds_0(1+\mu_{2a}) + rds_{14} + rds_{2a}}] \tag{7}$$

$$G = [\frac{gm_{4a}}{gm_{4b}}(\frac{gm_{4c}\mu_{18}}{gm_{4d} h.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}} - \frac{\mu_{1b}}{rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) + \frac{\mu_{14}}{rds_0(1+\mu_{2a}) + rds_{14} + rds_{2a}}] \tag{8}$$

For *C2* node also act in accordance with the above and its current equation will be:

$$I_y = gm_{3a} Vgs_{3a} + \frac{Vin_2 \mu_{1a} - Vin_1 \mu_{13}}{h.rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}} \tag{9}$$

That Vgs_{3a} and Vgs_{3c} from small-signal analysis can be written:

$$Vgs_{3a} = [\frac{1}{gm_{3b}} \| rds_{3b} \| rds_{3c} \| R_{16}](gm_{3c}Vgs_{3c} + \frac{Vin_1\mu_{2b} - Vin_2\mu_{16}}{h.rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}) \quad (10)$$

$$Vgs_{3c} = [\frac{1}{gm_{3d}} \| rds_{3d} \| R_{17}](\frac{Vin_2\mu_{1c} - Vin_1\mu_{17}}{h.rds_0(1+\mu_{1c}) + rds_{1c} + rds_{17}}) \quad (11)$$

Finally, we have:

$$I_y = Vin_2(N) - Vin_1(M) \quad (12)$$

And:

$$M = [\frac{gm_{3a}}{gm_{3b}}(\frac{gm_{3c}\mu_{17}}{gm_{3d}h.rds_0(1+\mu_{1c}) + (rds_{1c} + rds_{17})} - \frac{\mu_{2b}}{rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}) + \frac{\mu_{13}}{rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}}] \quad (13)$$

$$N = [\frac{gm_{3a}}{gm_{3b}}(\frac{gm_{3c}\mu_{1c}}{gm_{3d}h.rds_0(1+\mu_{1c}) + (rds_{1c} + rds_{17})} - \frac{\mu_{16}}{rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}) + \frac{\mu_{1a}}{rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}}] \quad (14)$$

Based on the equations (6) and (12), and considering the *Vin1* and *Vin2* coefficients in these two equations, it can be observed that if *Ix* and *Iy* become zero in Common mode, in which *Vin1* and *Vin2* are same-signed, CMRR will be infinite. On the other hand, in differential mode which input voltages *Vin1* and *Vin2* have different signs, the current transferred to the output block will have a significant amount which explains the satisfactory function of CMRR magnifier block in simulation. Condition for above-mentioned advantages to be true for *C1* and *C2* nodes are as follows:

For *C1* node:

$$\begin{cases} \mu_{18} = \mu_{2c} \\ \mu_{15} = \mu_{1b} \\ \mu_{14} = \mu_{2a} \end{cases} \quad (15)$$

And for *C2* node:

$$\begin{cases} \mu_{17} = \mu_{1c} \\ \mu_{16} = \mu_{2b} \\ \mu_{13} = \mu_{1a} \end{cases} \quad (16)$$

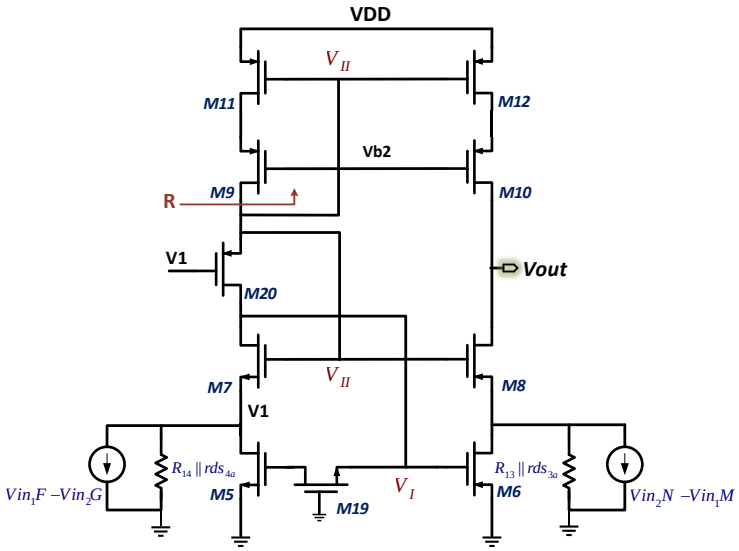


Figure 3. The small-signal equivalent circuit for output stage

$$Vgs_5 = Vgs_6 = V_I \tag{17}$$

V_1 can be calculated as follows:

$$V_1 = (gm_5 + Vin_1F - Vin_2G)[\mathrm{R}_{14} \| rds_{4a} \| rds_5 \| 1/gm_5] \tag{18}$$

And:

$$V_I = (\mathrm{V}_1 \mu_7 gm_5 - \frac{V_1 \mu_{20}}{rds_{20} + R(1+\mu_{20})})[1/gm_5 \| rds_{20} + \mathrm{R}(1+\mu_{20})] \tag{19}$$

By substituting V_1 at V_I , we have:

$$V_I = \frac{(Vin_1F - Vin_2G)[\frac{\mu_7}{gm_5} - \frac{\mu_{20}}{rds_{20} + R(1+\mu_{20})}]}{1 - gm_5[\frac{\mu_7}{gm_5} - \frac{\mu_{20}}{rds_{20} + R(1+\mu_{20})}]} = K_1(Vin_1F - Vin_2G) \tag{20}$$

Also, for V_{II} we can write:

$$V_{II} - V_1 = \frac{(Vin_1F - Vin_2G)\,1/gm_5}{1 - \mu_7 + \frac{\mu_{20}}{gm_5(rds_{20} + R(1+\mu_{20})}} = K_2(Vin_1F - Vin_2G) \tag{21}$$

Which R_z and R_K are equal to:

$$R_z = \frac{rds_{12} + rds_{10}}{1+\mu_{10}} \tag{22}$$

$$R_K = (R_{13} \| rds_{3a} \| rds_6)(1+\mu_8) \tag{23}$$

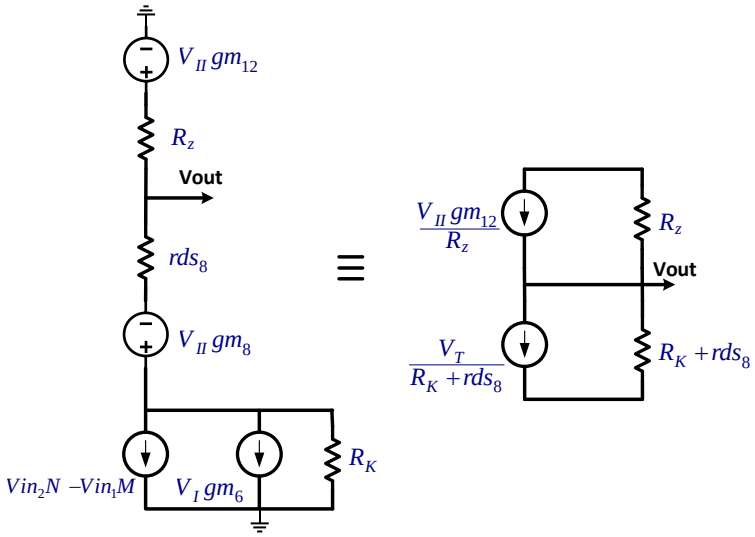


Figure 4. The small-signal analysis circuit to calculate *Vout*

Also:

$$\begin{aligned} V_T &= V_{II}\,gm_8 + R_K\,(gm_6 V_I + Vin_2 N - Vin_1 M) = K_2 gm_8 (Vin_1 F - Vin_2 G) \\ &+ K_1 R_K\,gm_6 (Vin_1 F - Vin_2 G) - R_K\,(Vin_1 M - Vin_2 N) \\ &= Vin_1 (K_2 gm_8 F + K_1 R_K\,gm_6 F - R_K M) - Vin_2 (K_2 gm_8 G + K_1 R_K\,gm_6 G - R_K N) \end{aligned} \tag{24}$$

According to Figure 4, *Vout* can be written as:

$$\begin{aligned} Vout &= (R_z \| R_K + rds_8)[\frac{V_{II}\,gm_{12}}{R_z} + \frac{V_T}{R_K + rds_8}] = \\ &(R_z \| R_K + rds_8) * \left[\begin{array}{l} Vin_1 (\frac{K_2 gm_8 F + K_1 R_K\,gm_6 F - R_K M}{R_K + rds_8} + \frac{K_2 gm_{12} F}{R_z}) - \\ Vin_2 (\frac{K_2 gm_8 G + K_1 R_K\,gm_6 G - R_K\ \mathrm{N}}{R_K + rds_8} + \frac{K_2 gm_{12} G}{R_z}) \end{array} \right] \end{aligned} \tag{25}$$

That *Ac* and *Ad* are as follows:

$$\begin{aligned} A_c &= \frac{Vout_c}{V_c} = (R_z \| R_K + rds_8) * \\ &\left[(\frac{K_2 gm_8 (F-G) + K_1 R_K\,gm_6 (F-G) - R_K\,(M-N)}{R_K + rds_8} + \frac{K_2 gm_{12} (F-G)}{R_z}) \right] \end{aligned} \tag{26}$$

$$\begin{aligned} A_d &= \frac{Vout_d}{\frac{V_d}{2}} = (R_z \| R_K + rds_8) * \\ &\left[(\frac{K_2 gm_8 (F+G) + K_1 R_K\,gm_6 (F+G) - R_K\,(M+N)}{R_K + rds_8} + \frac{K_2 gm_{12} (F+G)}{R_z}) \right] \end{aligned} \tag{27}$$

Now, we can calculate CMRR using equations (26) and (27).

$$CMRR = \frac{A_d}{A_c} = \frac{A(F+G) - B(M+N)}{A(F-G) - B(M-N)} \tag{28}$$

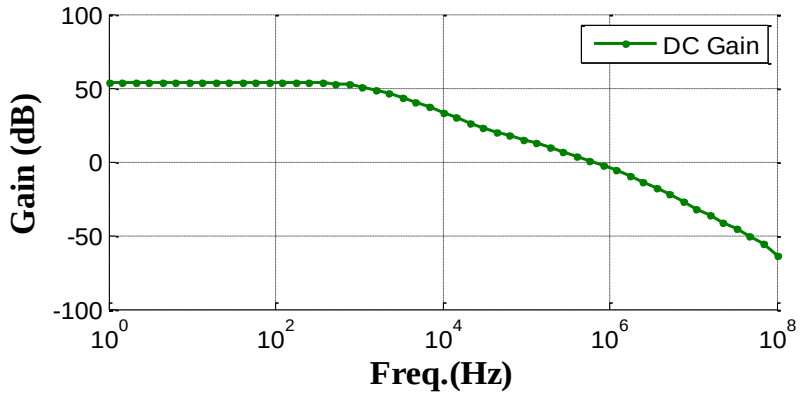
Where A and B are:

$$\begin{aligned} A &= R_Z\,(K_2 gm_8 + K_1 R_K\, gm_6) + K_2 gm_{12}(R_K + rds_8) \\ \mathrm{B} &= R_K\,.R_Z \end{aligned} \tag{29}$$

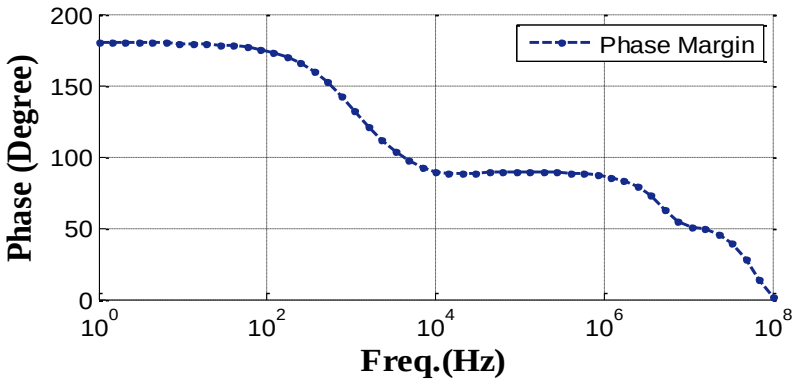
If F=G and M=N the denominator of CMRR approaches zero and theoretically infinite CMRR is obtained.

3. Simulation Results

To demonstrate the performance of low power low voltage CMRFC amplifier, this circuit is simulated in 180nm CMOS Technology. Cascode transistors which need high supply voltage for proper performance replace by transistors. Thus, proposed circuit supply voltage and consequently its power consumption gets low. In presented circuit with a supply voltage of 1.5v, Bias current is 7.2μA. Thus, power consumption is going to be 8.45μw which is a desirable value with respect to common RFC amplifiers for low power practical purposes. CMRFC amplifier gain is going to be 54.1dB because of removing common mode current by CMRR magnifier block which shows in Figure 5.



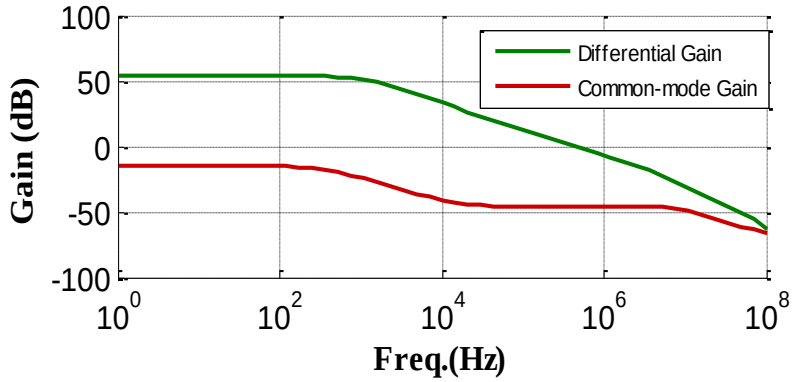
(a)



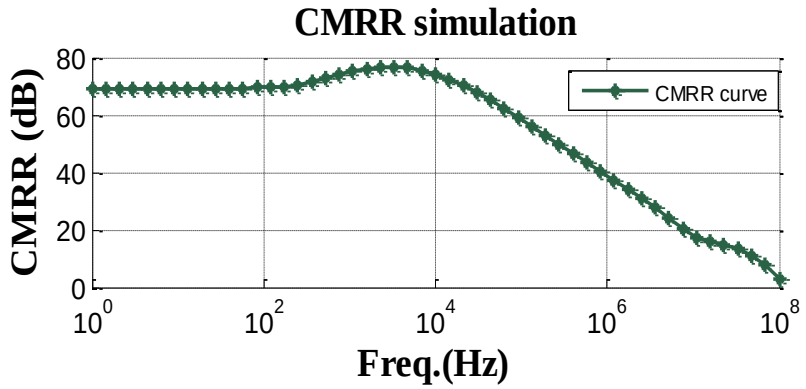
(b)

Figure 5. (a) Gain and (b) Phase margin simulation of CMRFC OTA

Differential and common mode gain simulation shows that according to equation (28) there is more amplification in differential mode and proper attenuation in common mode. Thus, the CMRR for this circuit is achieved 69.2 dB which is shown in Figure 6.



(a)



(b)

Figure 6. Simulated (a) differential and common mode gain, (b) CMRR

For comparison with other works, integrated noise analysis is done at a frequency of 1Hz to 6KHz. It is observed that the noise in this circuit is a little bit more than others, which can be possibly reduced by setting the transistor dimensions.

Monte Carlo and noise analysis is shown in Figure 7 and Figure 8, respectively. This show the qualitative performance amplifier has been proposed and its function properly.

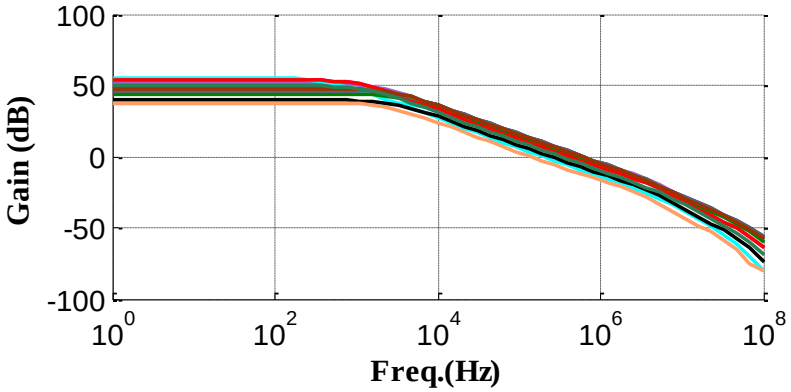


Figure 7. Monte Carlo analysis of proposed CMRFC OTA

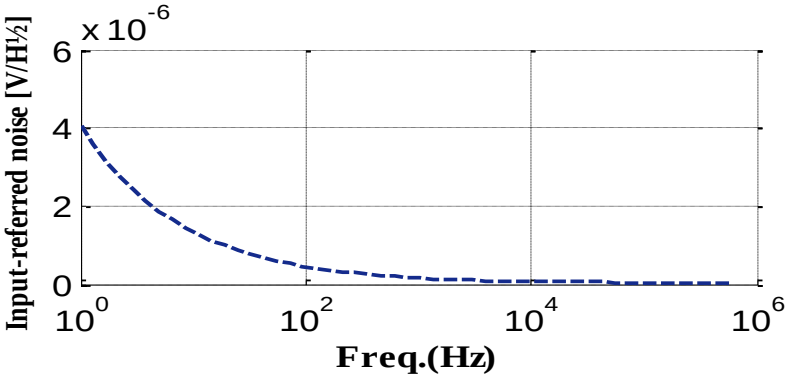


Figure 8. Input-referred noise of Low power CMRFC OTA

A comparison between the proposed CMRFC and other structures is presented in Table 1. Lower power consumption, bias current and voltage and high gain and CMRR are desirable features of this structure.

Table 1.Performance summary

Reference	Proposed	[13]	[14]	[15]	[16]	[17]
Technology [nm]	180	180	180	180	180	180
supply voltage [v]	1.5	1.8	±0.9	±0.9	1.8	1.8
Capacitive load [pF]	20	-	70	23	-	-
GBW [MHz]	0.62	0.58	10.7	0.57	9	-
DC Gain [dB]	54.1	70	80.5	67	48.6	42.78
Phase-margin [deg]	87.16	84	60	82	-	-
Bias current [μA]	7.2	7.9	23	8	6.11	7.57
DC power [μw]	8.45	14.2	41.4	14.5	11	13.64
CMRR [dB]	69.25	-	-	73.2	55	43.11
Input referred noise [μVrms]	13.67	-	30.8	-	5	-

4. Conclusion

A low power CMRFC amplifier using the CMRR magnifier block was presented in this paper. Cascode transistors which increase the supply voltage and power consumption were eliminated. Common mode current was strictly eliminated by CMRR magnifier block which yielded a relatively low power and high CMRR compared with other low power structures. The low power CMRFC OTA was simulated in 180nm CMOS technology utilizing a 1.5v

supply and 7.2μA bias current and 8.45μw DC power with 54.1dB gain and 69.25dB CMRR are achieved which made it suitable for high gain and low power applications.

References

[1] Saini, R., Sharma, K., & Sharma, R. (2022). A low-noise high-gain recycling folded cascode operational transconductance amplifier based on gate driven and quasi-floating bulk technique. Journal of Circuits, Systems and Computers, 31(06), 2250099.

[2] Sharma, K., & Sharma, R. (2019). Design considerations for effective neural signal sensing and amplification: a review. Biomedical Physics & Engineering Express, 5(4), 042001.

[3] Harrison, R. R. (2008). The design of integrated circuits to observe brain activity. Proceedings of the IEEE, 96(7), 1203-1216.

[4] Monfaredi, K., & Belghisazar, Y. (2018). Improved low voltage low power recycling folded fully differential cascode amplifier. TABRIZ Journal of electrical Engineering, 48(1), 327-334.

[5] Jos´e M. de la Rosa and Roc´ıo del R´ıo. (2013). CMOS Sigma-Delta Converters: Practical Design Guide. John Wiley & Sons.

[6] Assaad, R. S., & Silva-Martinez, J. (2009). The recycling folded cascode: A general enhancement of the folded cascode amplifier. IEEE Journal of Solid-State Circuits, 44(9), 2535-2542.

[7] Li, Y. L., Han, K. F., Tan, X., Yan, N., & Min, H. (2010). Transconductance enhancement method for operational transconductance amplifiers. Electronics letters, 46(19), 1321-1323.

[8] Yan, Z., Mak, P. I., & Martins, R. P. (2012). Double recycling technique for folded-cascode OTA. Analog integrated circuits and signal processing, 71, 137-141.

[9] Yosefi, G. (2019). The high recycling folded cascode (HRFC): A general enhancement of the recycling folded cascode operational amplifier. Microelectronics journal, 89, 70-90.

[10] Rashtian, M. (2022). Adaptive double recycling folded cascode amplifier. Analog Integrated Circuits and Signal Processing, 110(1), 165-174.

[11] Akbari, M., Biabanifard, S., & Asadi, S. (2015). Input referred noise reduction technique for trans-conductance amplifiers. Electrical and Computer Engineering: An International Journal (ECIJ), 4(4), 11-22.

[12] Voo, T., & Toumazou, C. (1995). High-speed current mirror resistive compensation technique. Electronics Letters, 31(4), 248-250.

[13] Choi, G., Heo, H., You, D., Kim, H., Nam, K., Yoo, M., ... & Ko, H. (2021). A low-power, low-noise, resistive-bridge microsensor readout circuit with chopper-stabilized recycling folded cascode instrumentation amplifier. Applied Sciences, 11(17), 7982.

[14] Yen, A., & Blalock, B. J. (2020, August). A High Slew Rate, Low Power, Compact Operational Amplifier Based on the Super-Class AB Recycling Folded Cascode. In 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS) (pp. 9-12). IEEE.

[15] Pourashraf, S., Ramirez-Angulo, J., Lopez-Martin, A. J., & Carvajal, R. G. (2017). Super class AB OTA without open-loop gain degradation based on dynamic cascode biasing. International Journal of Circuit Theory and Applications, 45(12), 2111-2118.

[16] Kmon, P., & Gryboś, P. (2013). Energy efficient low-noise multichannel neural amplifier in submicron CMOS process. IEEE Transactions on Circuits and Systems I: Regular Papers, 60(7), 1764-1775.

[17] Sam, D. S., Paul, P. S., & Jayanthi, D. (2021, March). A Novel architecture of a Low Power Folded Cascode OTA in 180nm CMOS process. In 2021 7th International Conference on Advanced Computing and Communication Systems (ICACCS) (Vol. 1, pp. 95-99). IEEE.